

CLIPPEDIMAGE= JP405251647A
PAT-NO: JP405251647A
DOCUMENT-IDENTIFIER: JP 05251647 A
TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUBN-DATE: September 28, 1993

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APPL-NO: JP04048705

APPL-DATE: March 5, 1992

INT-CL (IPC): H01L027/06; H01L021/76 ; H01L021/80

US-CL-CURRENT: 257/371,257/372

ABSTRACT:

PURPOSE: To uniform element characteristics by suppressing a lateral spread of a well by a shallow well between different kinds of elements to shorten the element isolation width and by connecting wells in desired regions in the same kinds of elements in a title device including a MOSFET.

CONSTITUTION: An n-type Si substrate 1 is overlaid with a plurality of nMOSFETs 41a, 41b. 7a-7i are element isolation insulating layers, and 11a-11d MOSFET gate electrodes. Between p-wells 5c, 5a and 5a, 5b, that is, under element isolation insulating layers 7b and 7c exist p<SP>+</SP> semiconductor layers 9b and 9c which connect these wells. The position of a pn junction between these

p<SP>+</SP> semiconductor and the n-type Si substrate 1 is deeper than that of a pn junction between the p-wells 5c, 5a, and 5b and the n-type Si substrate 1, where wells are connected by low resistances. An element isolation insulating layer 7d of pMOSFETs 42a, 42b that are adjacent different kinds of elements suppresses a lateral spread of a well and shortens the element isolation width.

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2	865	(257/506,509,510).CCLS.	USPAT	2002/05/31 14:48
5	540	257/208	USPAT	2002/05/31 15:07
8	1465	semiconductor adj device and Mitsubishi and isolation	USPAT; JPO; DERWENT	2002/05/31 15:15
9	10	semiconductor adj device and Mitsubishi and complete adj isolation	USPAT; JPO; DERWENT	2002/05/31 15:19
10	49	semiconductor adj device and complete adj isolation and partial	USPAT; JPO; DERWENT	2002/05/31 15:23
11	40	soi and complete adj isolation and partial	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/31 15:24
-	855	(257/347).CCLS.	USPAT	2002/05/31 09:22
-	2999	semiconductor and soi and (power or ground)	USPAT	2002/05/31 09:18
-	289	(257/207).CCLS.	USPAT	2002/05/31 10:32
-	9	("5399507" "5484738" "5712205" "5728620" "5780352" "5858842" "5985733" "6221737" "6271070").PN.	USPAT	2002/05/31 11:22